In re Patent Application of
ERRATICO
S rial No. **09/899,573**
Filed: **JULY 5, 2001**

In the Claims:

This listing of claims replaces all prior versions and listing of claims in the application.

1-11. (canceled).

12. (currently amended) ~~An~~ A Bipolar-CMOS-DMOS (BCD) integrated circuit ~~structure~~ comprising:

a substrate having a first conductivity type;

an epitaxial layer on said substrate and having the first conductivity type and a conductivity less than a conductivity of said substrate;

first and second regions in said epitaxial layer each having a second conductivity type opposite the first conductivity type, said first and second regions extending from a surface of said epitaxial layer opposite said substrate into said epitaxial layer to form respective first and second normally reverse-biased junctions therewith;

the first region defining a power section integrated in said epitaxial layer, and the second region defining a signal processing section integrated in said epitaxial layer, at least one of said power section and said signal processing section including at least one of a bipolar transistor and a DMOS transistor;

first and second electrodes for independently biasing the first and second junctions, respectively; and

an isolating element positioned between said first and said second regions and extending from the surface of said

epitaxial layer at least as far as a top surface of said substrate for reducing an injection of current through said epitaxial layer from said first region to said second region when the first junction is biased to cause the injection of current ~~and second junctions are oppositely biased~~, said isolating element comprising a dielectric material adjacent said epitaxial layer and polycrystalline silicon spaced apart from said epitaxial layer by said dielectric material, said isolating element also terminating above a bottom surface of said substrate.

13. (currently amended) The Bipolar-CMOS-DMOS (BCD) integrated circuit ~~structure~~ according to Claim 12 wherein said isolating element at least partially surrounds said first region.

14. (currently amended) The Bipolar-CMOS-DMOS (BCD) integrated circuit ~~structure~~ according to Claim 12 wherein said integrated circuit ~~structure~~ is formed on a semiconductor chip; and wherein said isolating element has a length substantially equal to a width of the semiconductor chip and divides the semiconductor chip into two portions each respectively including said first region and said second region.

15. (currently amended) The Bipolar-CMOS-DMOS (BCD) integrated circuit ~~structure~~ according to Claim 12 wherein the first conductivity type is P type.

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16. (currently amended) The Bipolar-CMOS-DMOS (BCD) integrated circuit ~~structure~~ according to Claim 12 wherein said ~~first region~~ power section comprises a power transistor for controlling an inductive load.

17. (currently amended) ~~An~~ A Bipolar-CMOS-DMOS (BCD) integrated circuit ~~structure~~ comprising:

a substrate having a first conductivity type;

an epitaxial layer on said substrate and having the first conductivity type and a conductivity less than a conductivity of said substrate;

first and second regions in said epitaxial layer each having a second conductivity type opposite the first conductivity type, said first and second regions extending from a surface of said epitaxial layer opposite said substrate into said epitaxial layer to form respective first and second normally reverse-biased junctions therewith;

the first region defining a power section integrated in said epitaxial layer, and the second region defining a signal processing section integrated in said epitaxial layer, at least one of said power section and said signal processing section including at least one of a bipolar transistor and a DMOS transistor;

first and second electrodes for independently biasing the first and second junctions, respectively; and

an isolating element positioned between said first and said second regions and extending from the surface of said

epitaxial layer at least as far as a top surface of said substrate for reducing an injection of current through said epitaxial layer from said first region to said second region when the first junction is biased to cause the injection of current ~~and second junctions are oppositely biased~~, said isolating element partially surrounding at least one of said first and second regions, said isolating element also terminating above a bottom surface of said substrate.

18. (currently amended) The Bipolar-CMOS-DMOS (BCD) integrated circuit ~~structure~~ according to Claim 17 wherein said isolating element comprises a dielectric material.

19. (currently amended) The Bipolar-CMOS-DMOS (BCD) integrated circuit ~~structure~~ according to Claim 18 wherein said isolating element further comprises polycrystalline silicon.

20. (currently amended) The Bipolar-CMOS-DMOS (BCD) integrated circuit ~~structure~~ according to Claim 17 wherein the first conductivity type is P type.

21. (currently amended) The Bipolar-CMOS-DMOS (BCD) integrated circuit ~~structure~~ according to Claim 17 wherein said ~~first region~~ power section comprises a power transistor for controlling an inductive load.

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22. (currently amended) ~~An~~ A Bipolar-CMOS-DMOS (BCD) integrated circuit ~~structure~~ formed on a semiconductor chip and comprising:

a substrate having a first conductivity type;

an epitaxial layer on said substrate and having the first conductivity type and a conductivity less than a conductivity of said substrate;

first and second regions in said epitaxial layer each having a second conductivity type opposite the first conductivity type, said first and second regions extending from a surface of said epitaxial layer opposite said substrate into said epitaxial layer to form respective first and second normally reverse-biased junctions therewith;

the first region defining a power section integrated in said epitaxial layer, and the second region defining a signal processing section integrated in said epitaxial layer, at least one of said power section and said signal processing section including at least one of a bipolar transistor and a DMOS transistor;

first and second electrodes for independently biasing the first and second junctions, respectively; and

an isolating element positioned between said first and said second regions and extending from the surface of said epitaxial layer at least as far as a top surface of said substrate for reducing an injection of current through said epitaxial layer from said first region to said second region when the first junction is biased to cause the injection of current ~~and second junctions are oppositely biased~~, said

isolating element having a length substantially equal to a width of the semiconductor chip and dividing the semiconductor chip into two portions each respectively including said first and said second regions, said isolating element also terminating above a bottom surface of said substrate.

23. (currently amended) The Bipolar-CMOS-DMOS (BCD) integrated circuit ~~structure~~ according to Claim 22 wherein said isolating element comprises a dielectric material.

24. (currently amended) The Bipolar-CMOS-DMOS (BCD) integrated circuit ~~structure~~ according to Claim 23 wherein said isolating element further comprises polycrystalline silicon.

25. (currently amended) The Bipolar-CMOS-DMOS (BCD) integrated circuit ~~structure~~ according to Claim 22 wherein the first conductivity type is P type.

26. (currently amended) The Bipolar-CMOS-DMOS (BCD) integrated circuit ~~structure~~ according to Claim 22 wherein said ~~first region~~ power section comprises a power transistor for controlling an inductive load.